SILICON IP

HIGH SPEED INTERFACE: PCIE GEN 6

Ultra-high bandwidth link for next-generation compute systems

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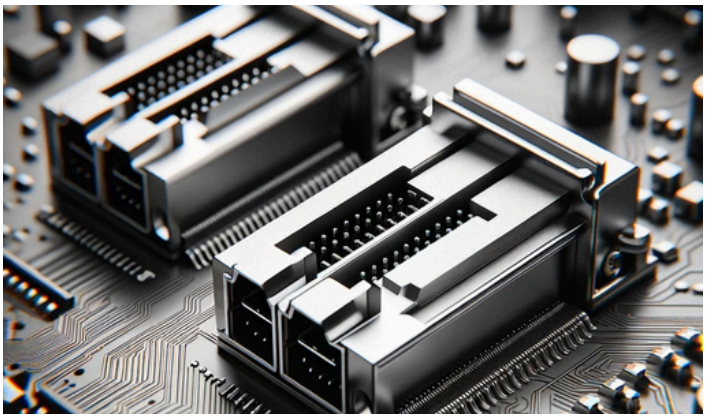
OVERVIEW

PCI Express (PCIe) Gen 6 is the latest evolution in the PCIe standard, delivering up to 64 GT/s per lane with PAM4 signaling and FLIT-based encoding. It supports a raw bandwidth of up to 256 GB/s in a 16-lane configuration, making it ideal for data-intensive applications such as AI/ML training, hyperscale data centers, and high-performance computing (HPC). With the introduction of Forward Error Correction (FEC), low-latency flow control, and backward compatibility with Gen 1–5, PCIe Gen 6 enables scalable and efficient interconnects between CPUs, GPUs, SSDs, accelerators, and switches. The interface is optimized for latency-sensitive and high-throughput workloads in advanced SoC and multi-die system architectures.



KEY FEATURES

64 GT/s per Lane Using PAM4 Signaling

- Doubles the bandwidth of PCIe Gen 5 with 4-level pulse amplitude modulation, enabling ultra-fast data transfer.

FLIT Mode with Low-Latency FEC

- Implements flow control units and lightweight FEC to maintain high efficiency and low bit error rates at elevated speeds.

Backward Compatibility

- Maintains support for Gen 1 through Gen 5 devices, ensuring smooth integration into legacy ecosystems.

Raw Bandwidth up to 256 GB/s (x16)

- Provides unmatched throughput across 16-lane links, critical for AI accelerators, networking, and storage subsystems.

Low Latency Path Optimization

- Introduces minimal encoding overhead and efficient buffer management for real-time workloads.

Scalable Lane Configurations

- Supports x1, x4, x8, and x16 configurations, adaptable to embedded, edge, and high-end compute environments.

Advanced Error Handling

- Integrates CRC, FEC, and flow control mechanisms to ensure robust link stability and error resilience.

Multi-Die and Chiplet Interoperability

- Suitable for disaggregated architectures, enabling high-bandwidth chip-to-chip and inter-die communication.

PIPE 6.x and PHY Layer Interface Compliance

- Compatible with latest PIPE and SerDes technologies for simplified integration and PHY abstraction.

Power Management Enhancements

- Supports advanced L0p, L1 substates, and dynamic link equalization to optimize power consumption.

USB 3.2 APPLICATIONS

High-Performance Computing (HPC)

- Delivers the bandwidth needed for massive parallel compute systems, enabling fast communication between CPUs, GPUs, memory, and storage in exascale architectures.

Artificial Intelligence / Machine Learning

- Accelerates training and inference by providing low-latency, high-bandwidth interconnects between AI accelerators, memory systems, and host processors.

Data Centers and Cloud Infrastructure

- Supports NVMe SSDs, accelerators, smart NICs, and interconnect fabrics for optimized workload distribution and data throughput.

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Networking and 5G Infrastructure

- Enables rapid packet processing and switching in next-gen routers, baseband units, and network interface cards with high I/O demand.

Chiplet-Based SoC Designs

- Ideal for inter-chiplet communication with scalable, high-speed interfaces supporting disaggregated system architectures.

Storage Subsystems

- Enhances PCIe-based NVMe SSD performance with ultra-fast sequential and random read/write access, key for tiered storage models.

Automotive and Edge Computing

- Supports compute-intensive in-vehicle systems and edge servers with real-time data transfer between sensors, inference modules, and host platforms.

Scientific and Industrial Systems

- Provides deterministic data rates and low latency links in simulation systems, real-time control, and industrial automation workloads.

PCIE GEN 6 ARCHITECTURE

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