SILICON IP

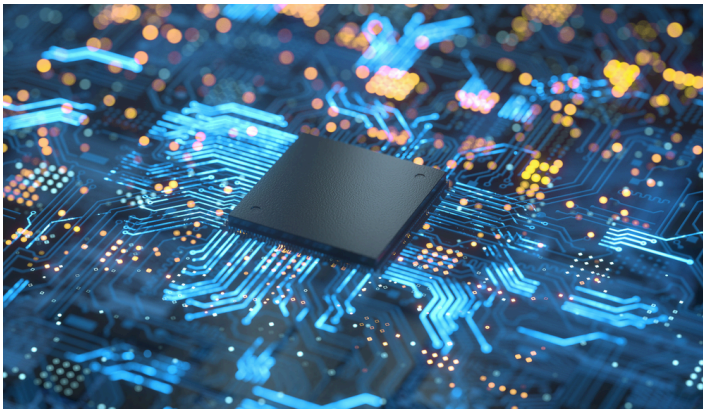
MEMORY CONTROLLER: DDR5 CONTROLLER

High-bandwidth memory controller for next-gen compute systems

For sales, please contact info@xtremesilica.com

OVERVIEW

DDR5 (Double Data Rate 5) is the latest generation of synchronous DRAM, offering significantly higher bandwidth, capacity, and power efficiency compared to DDR4. The DDR5 controller IP facilitates integration of this advanced memory standard into SoCs and FPGAs, providing a robust interface for high-performance computing, AI/ML accelerators, and enterprise-grade systems. With support for speeds exceeding 6400 MT/s, dual 32-bit subchannels per DIMM, and in-built Decision Feedback Equalization (DFE), the DDR5 controller delivers higher memory throughput with improved signal integrity. It is optimized for multi-core architectures and supports advanced memory scheduling, ECC, and multiple DIMMs per channel for scalable performance.



KEY FEATURES

Support for Up to 6400+ MT/s Data Rates

- Enables ultra-high-speed data access for memory-intensive applications, critical for AI, HPC, and real-time analytics.

Dual Independent 32-bit Subchannels

- Improves parallelism and memory access granularity, reducing latency and increasing effective bandwidth.

On-Die ECC and Inline Parity Support

- Enhances reliability and fault tolerance with integrated error detection and correction at the memory level.

Configurable Memory Scheduling Algorithms

- Advanced scheduler supports FR-FCFS, reordering, and prioritization to optimize memory efficiency and QoS.

Multi-Rank and Multi-DIMM Support

- Compatible with RDIMMs, UDIMMs, and 3DS DIMMs, allowing flexible scalability for server and embedded platforms.

DFE and CA/Command Bus Training Support

- Ensures signal integrity and link robustness using adaptive equalization and training features.

Low Power Operation Modes

- Includes support for deep power-down, clock gating, and self-refresh, enhancing energy efficiency.

AXI/Native Interface Options

- Supports standard AMBA AXI protocol or native interface for seamless SoC integration.

Secure Memory Access Hooks

- Optionally integrates memory region protection and access control features for security-sensitive workloads.

Timing Closure Assistance and Calibration

- Built-in PHY interface support and automated training improve system bring-up and reduce time-to-market.

DDR5 Controller Applications

High-Performance Computing (HPC)

- Maximizes memory throughput for compute nodes and exascale platforms, where DDR5's bandwidth accelerates large-scale simulations and modeling.

Artificial Intelligence and Machine Learning

- Feeds high-speed data to inference engines and neural networks, enabling faster training cycles and real-time predictions in edge and cloud AI.

Data Centers and Cloud Servers

- Provides high-density, low-latency memory solutions for virtualized environments, database workloads, and memory-hungry applications.

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Enterprise Storage Systems

- Optimizes caching and buffer layers in SSD controllers, RAID systems, and NVMe-oF setups, ensuring consistent high-speed data flows.

5G and Network Infrastructure

- Supports high-throughput packet processing and routing by offering scalable memory access for control plane and user plane functions.

Graphics and Visualization

- Delivers memory bandwidth needed by integrated GPUs and visualization engines for rendering, encoding, and real-time playback.

Automotive ADAS Systems

- Enhances responsiveness of ADAS platforms, supporting large sensor data buffers and compute modules in autonomous driving stacks.

Embedded and Industrial Computing

- Integrates into industrial controllers and automation platforms requiring deterministic latency and wide temperature-grade memory access.

DDR5 CONTROLLER ARCHITECTURE

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